

Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A LEAKAGE CURRENT CUTOFF CIRCUIT, CONSTRUCTED USING MT-CMOS, FOR REDUCING STANDBY LEAKAGE CURRENT

Inventor's Name: MIYAGI Application No.: NEW Docket No.: 100021-00133

$\frac{2}{20}$

Fig. 2A

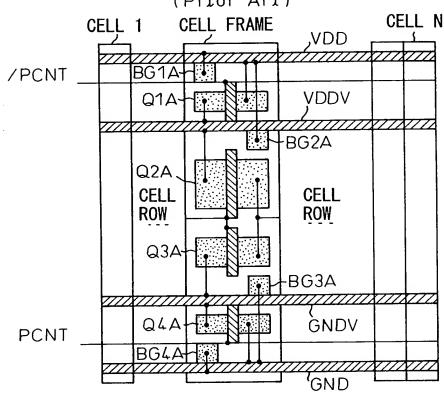
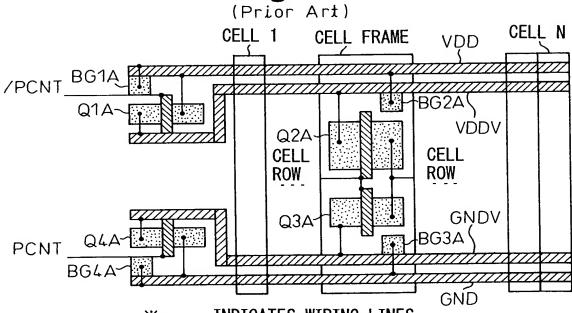
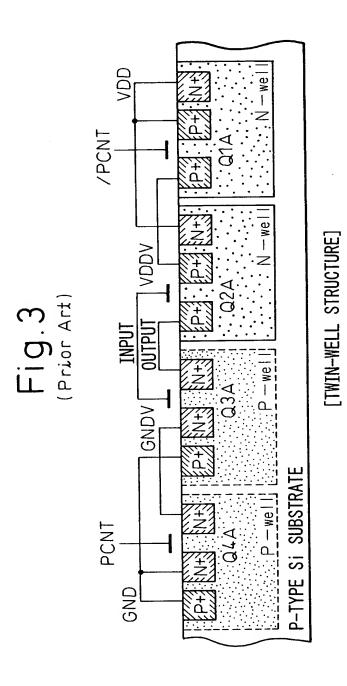


Fig. 2B



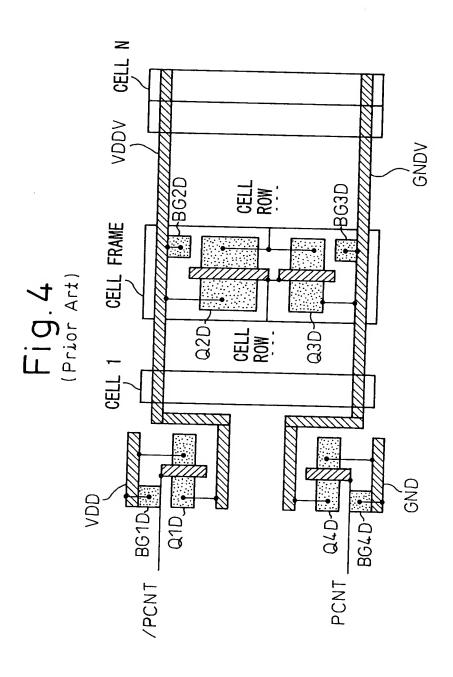
* INDICATES WIRING LINES AND THEIR CONNECTIONS

 $\frac{3}{20}$

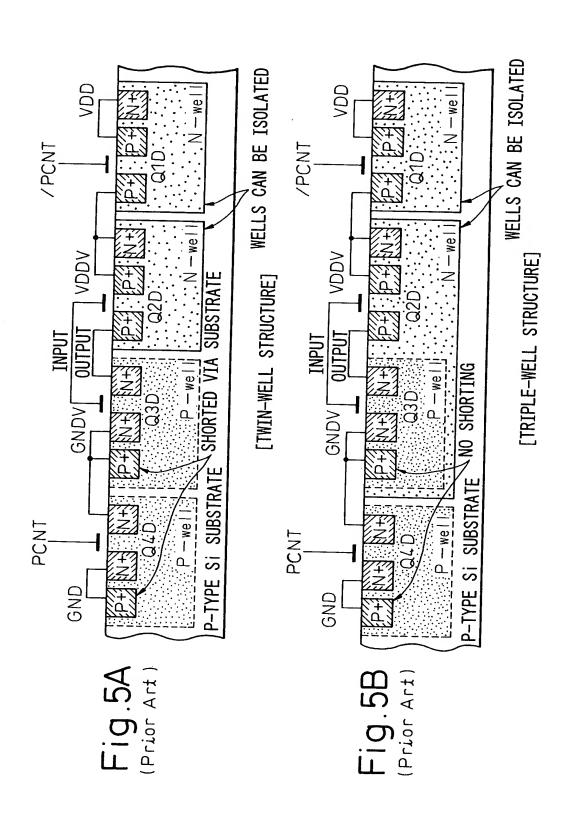


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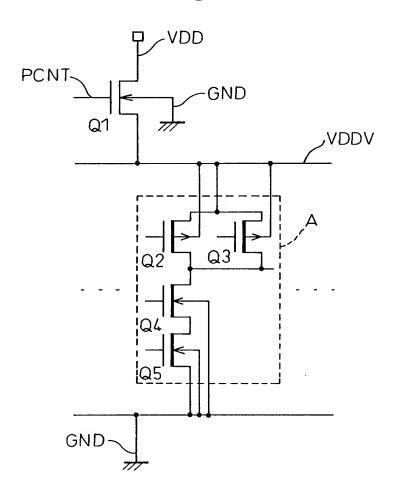


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Fig.6

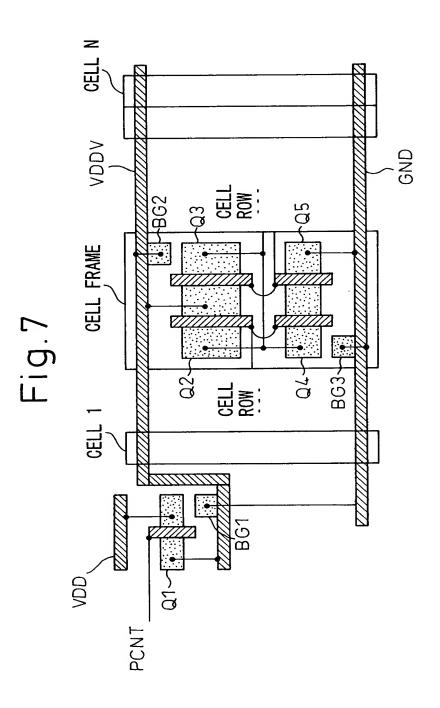


→
High-Vth NMOSFET →
Low-Vth PMOSFET

→
Low-Vth NMOSFET

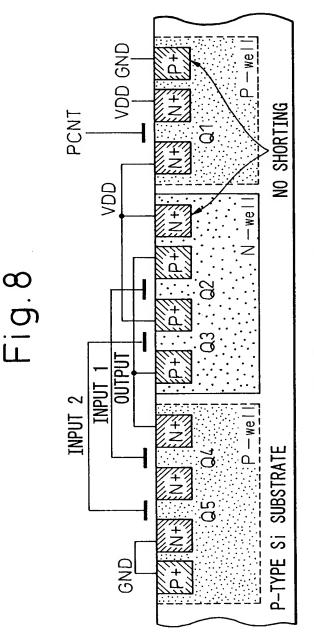
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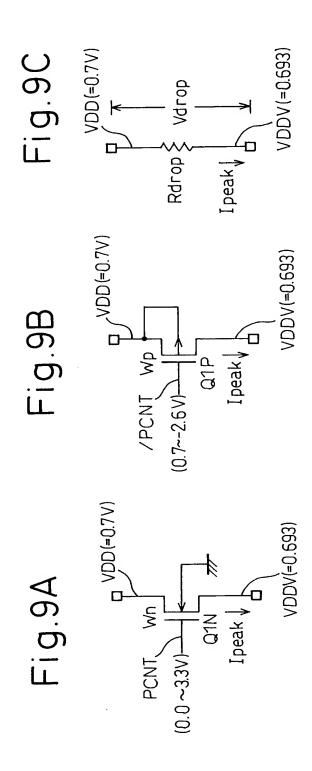
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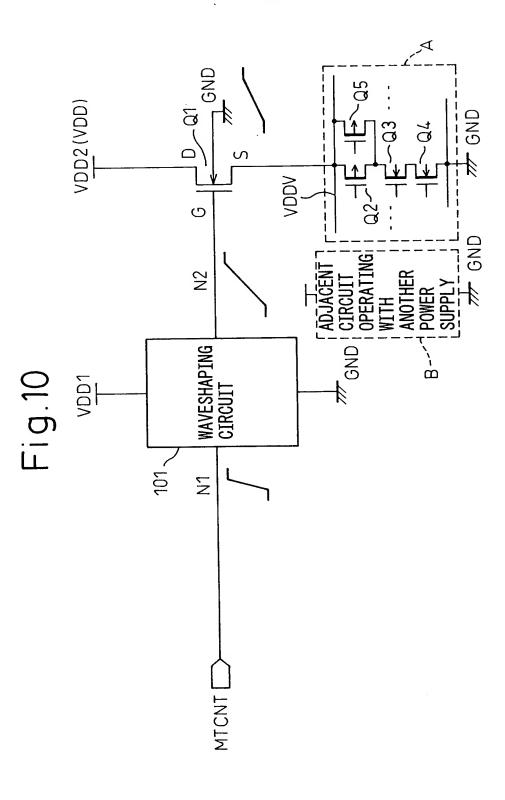
[TWIN-WELL STRUCTURE]

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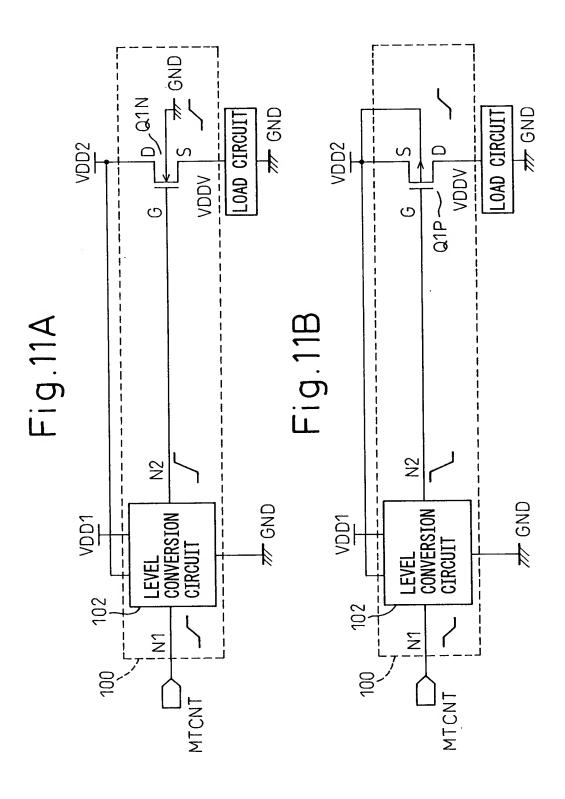
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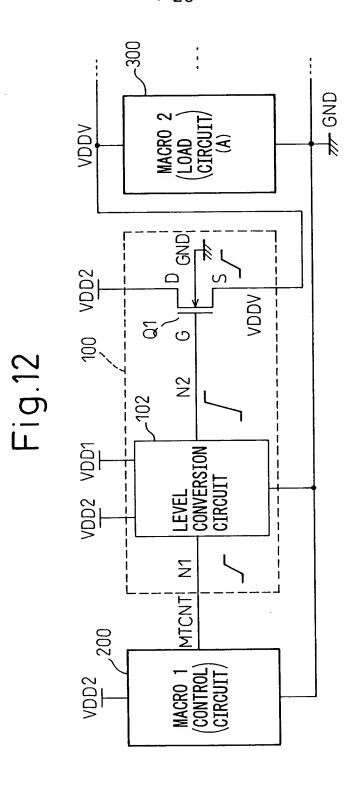
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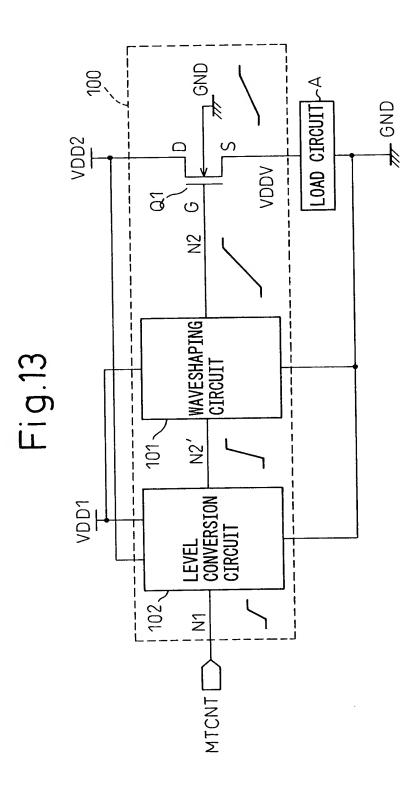
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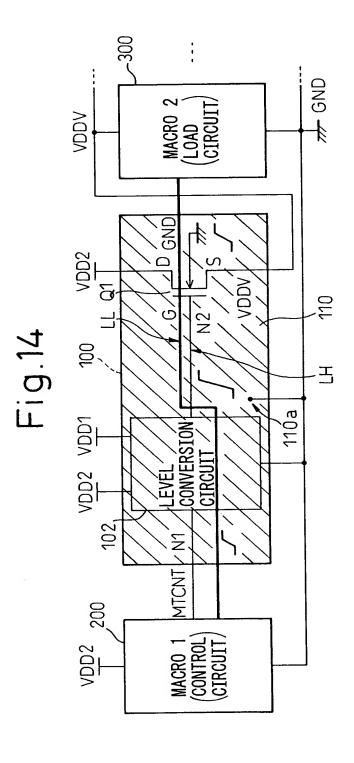


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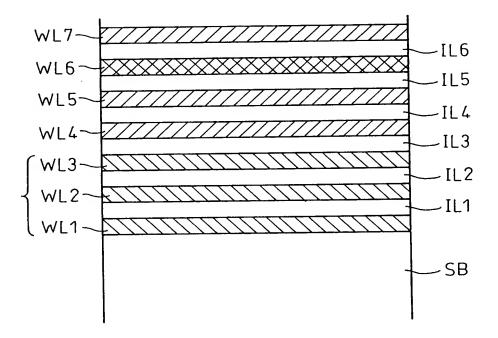
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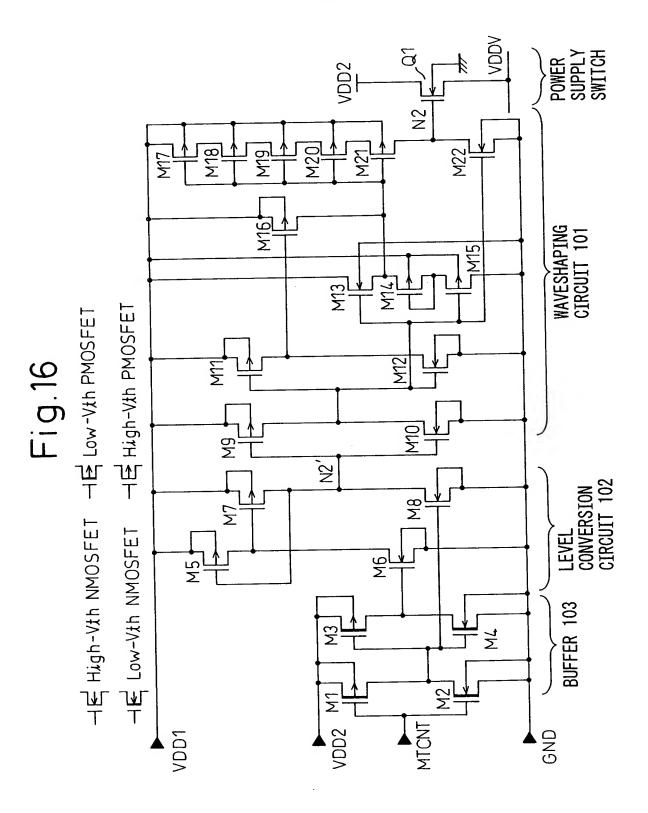
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Fig.15

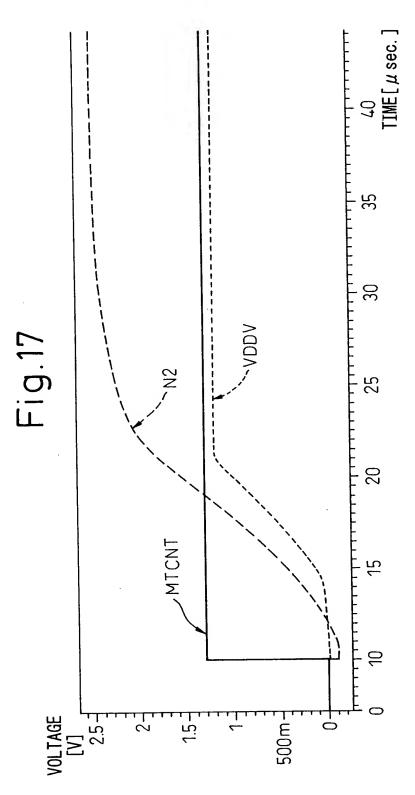


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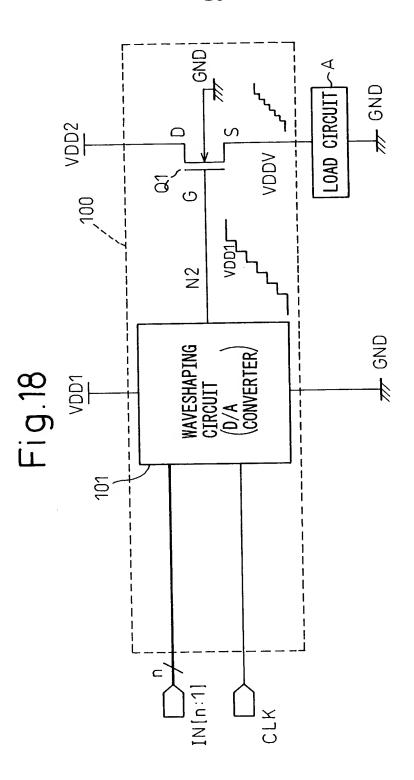
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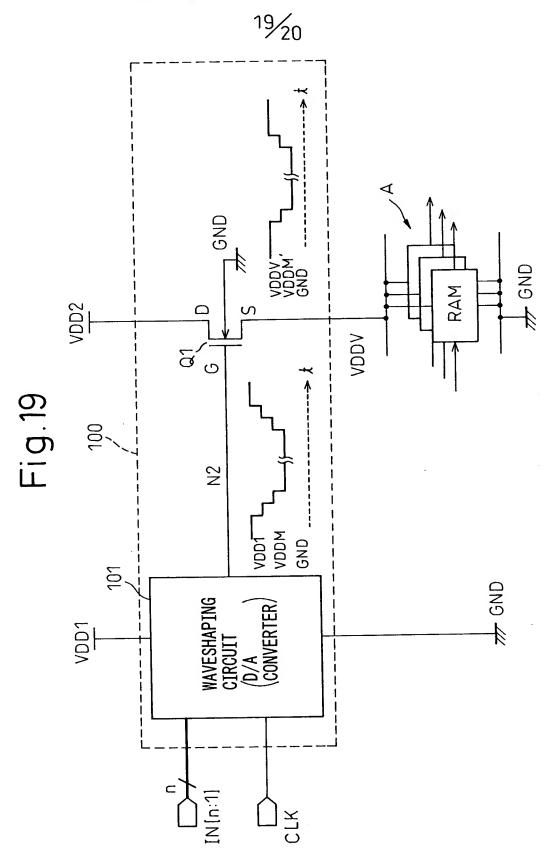






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